WHAT IS CLAIMED IS:

1. A memory device comprising:

a memory cell array block comprising pairs of memory cells, each being composed of a memory cell and a complementary memory cell and disposed at intersections of rows and columns, in which first and second memory cells and first and second complementary memory cells are connected to a first wordline arranged in the row direction, third and fourth memory cells and third and fourth complementary memory cells are connected to a second wordline, the first and third memory cells are adjacently disposed between the first and second wordlines, the second and fourth memory cells are adjacently disposed therebetween, the first and second complementary memory cells are adjacently disposed therebetween, and the third and fourth complementary memory cells are adjacently disposed therebetween;

a first sense amplifier disposed over the memory cell array block;

a second sense amplifier disposed under the memory cell array block;

a first switch for connecting bitlines coupled to the first memory cell and the first complementary memory cell with the first sense amplifier and connecting bitlines coupled to the second memory cell and the second complementary memory cell with the second sense amplifier; and

a second switch for connecting bitlines coupled to the third memory cell and the third complementary memory cell with the first sense amplifier and connecting bitlines coupled to the fourth memory cell and the fourth complementary memory cell with the second sense amplifier.

2. The memory device of claim 1, characterized in that the pairs of the memory cells are further arranged such that the first and second memory cells and the first and second complementary memory cells are interleaved and the third and fourth memory cells and the third and fourth complementary memory cells are also interleaved.

3. The memory device of claim 1, characterized in that when the first wordline is enabled to connect the first memory cell and the first complementary memory cell with the first sense amplifier and connect the second memory cell and the second complementary memory cell with the second sense amplifier, the third and fourth memory cells and third and fourth complementary memory cells, which are coupled to the second wordline, are set to a ground voltage level.

4. A memory device, comprising:

an array of unit memory cells, each unit memory cell comprising a memory cell and a complementary cell;

bitlines arranged such that a first and a third unit memory cells are connected to a first bitline, and a second and a third unit memory cells are connected to a second bitline, wherein the complementary cell of each unit memory cell is connected to a complementary bitline to the bitline connected to the memory cell;

sense amplifiers arranged adjacent the array; and

switches arranged such that the first and third bitlines are controlled by a first switch and the second and fourth bitlines are controlled by a second switch to selectively connect the bitlines to the sense amplifiers.

5. The memory device of claim 4, the first unit memory cell and the second memory cell being arranged in an interleaved fashion, and the third unit memory cell and the fourth unit memory cell being interleaved.

6. A method of reading a memory cell, the method comprising:

enabling a first wordline;

turning on a first switch connected to the first wordline;

transmitting data from a first unit memory cell to a first sense amplifier using a first bitline; and

transmitting data from a second unit memory cell to a second sense amplifier using the first bitline.

7. The method of claim 6, the method further comprising setting a second bitline and a third bitline to a ground voltage.